

**Datasheet**

**DBM3Cxx**

**Cyclone III NIOS II System Module**



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### Revisions

Revision	Remark	Date
1.00	Initial Version	14.10.2008
1.01	Additional Pin Information for Baseboard	28.10.2008
1.02	There is a bug in the Version 1.0 Boards. The MDIO Signal for the Ethernet MAC does not have a pull-up resistor. A workaround is to use an internal pull up inside the FPGA. In the Assignment Editor select Weak Pullup for the EMDIO Signal. Will be changed in Board Rev. 1.1	21.11.2008
1.03	There is a second bug in the Board Version 1.0. The 1.8V power generation of the Marvell Ethernet PHY is erroneous. U12 has interchange Collector and Emitter. Nevertheless, the Powersupply is working correct. Will be changed in Board Rev. 1.1	30.03.2009
1.04	Error in documentation, Module contains 512Kx32 = 2Mbyte SRAM	08.02.2010

## Ordering Information

### DBM3Cxx general features

- Cyclone III FPGA 3C16, 3C40, 3C55, 3C80
- EPCS64 64Mbit Configuration Device
- IS61WV51232 512Kx32bit (2Mbyte) SRAM – 10ns
- IS42S32160 16Mx32bit (64MByte) SDRAM
- S29GL256GP 16Mx16bit (32Mbyte) Nor Flash
- 88E1119R Gigabit Ethernet Phy
- 6 LVDS Output Channel
- 6 LVDS Input Channel
- 65 I/O Signals(3.3V)
- 6 Input Signals (3.3V)
- 1.2V / 2.5V Core Power Supply
- 1.27mm Module connector

### DBM3C16

- Equipped with Cyclone III FPGA EP3C16F484C7N

### DBM3C40

- Equipped with Cyclone III FPGA EP3C40F484C7N

### DBM3C55

- Equipped with Cyclone III FPGA EP3C55F484C7N

### DBM3C80

- Equipped with Cyclone III FPGA EP3C80F484C7N

### DBM\_CIII\_Base

- 95 – 240V Power Supply
- 3.3V Power supply for Module
- Pin header for all signals
- JTAG Interface
- RS232 / Sub-D 9
- Micro SD Card Socket

### DBM\_3C40\_Start

- DBM3C40 module
- DBM\_CIII\_Base
- Altera USB-Blaster
- NIOS II License
- Quartus II Web Edition
- Reference Designs

## DBM3Cxx – Cyclone III NIOS II System Module

### Customized Modules

We can deliver this module with customized FPGAs and peripherals.

## DBM3Cxx – Cyclone III NIOS II System Module

### Introduction

The DBM3Cxx NIOS II System Module is a ready to use module containing all the required parts for a complete Processor Module.

- Several Cyclone III devices are available
- EPCS64 configuration device
- Marvel 88E1119 Gigabit Ethernet Phy
- 2x6 channel LVDS links
- Up to 64Mbyte SDRAM
- 2Mbyte SRAM
- Up to 128Mbyte Nor Flash
- 65 I/O Signals
- 6 Input Signals
- on board 1.2V and 2.5V power supply
- Dimension: 36 x 70mm

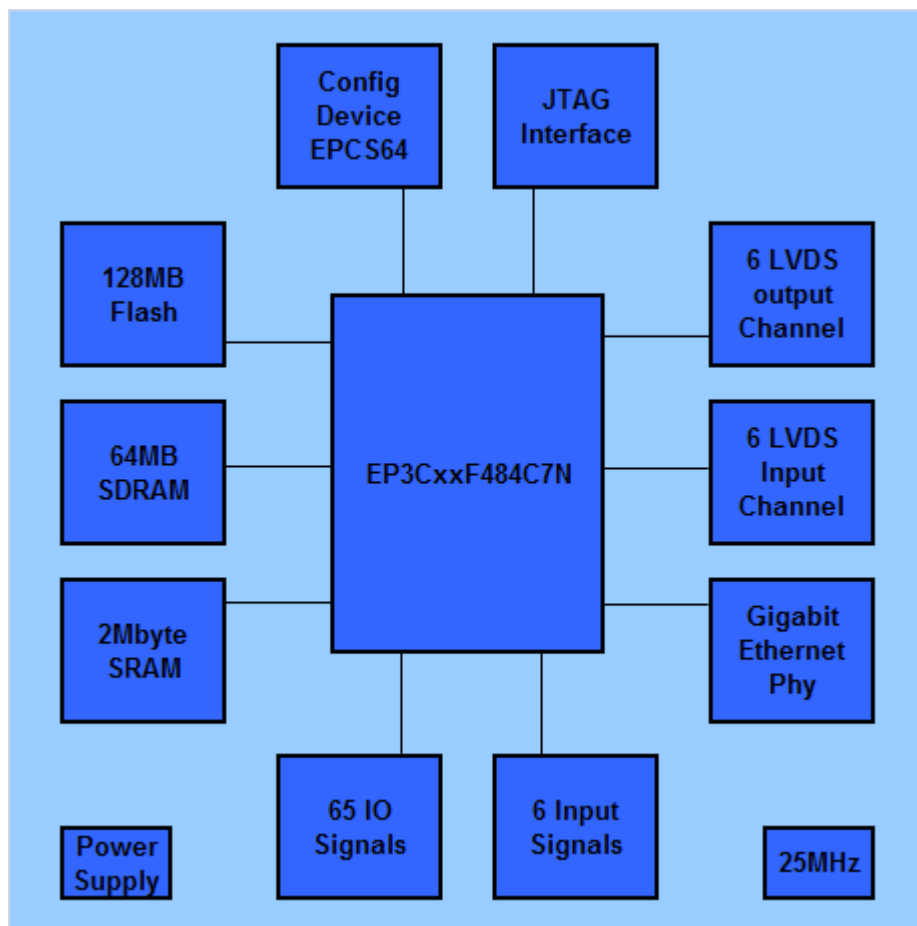


figure 1

### Installation

For installing the documentation, applications and reference designs from the DVD, just insert the DVD in the DVD drive of your computer. Then you get a start screen:

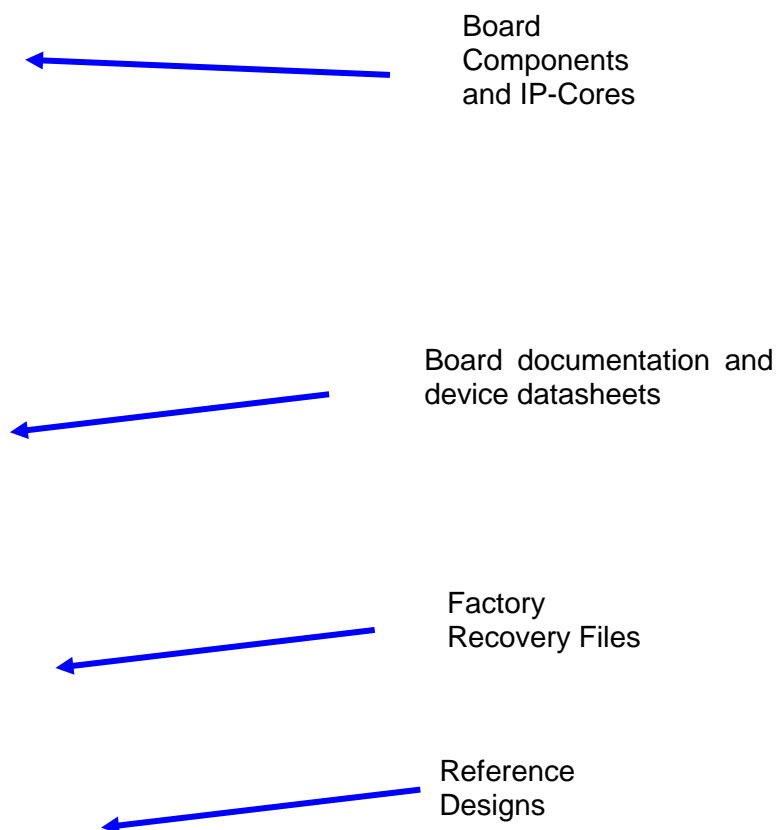
- you can read the documentation (PDF)
- you can install the applications and reference designs on your computer.

Please install the applications in the following sequence:

- install the Quartus<sup>®</sup> Web Edition
- start the Quartus<sup>®</sup>II software to register the current version
- install Nios<sup>®</sup>II Version
- install the reference designs.
- request a Quartus<sup>®</sup>II Web Edition license

**Attention: Make sure that there is no blank in the path! (E.g. \My documents)**

When you have finished the installation of the reference designs you can find the following folders on your hard disk:



## Getting started

### *Documentation*

The complete documentation of the board, the reference designs, IP functions and the on-board devices are stored in the documentation directory of the Altera® Nios® II directory e.g. C:\Altera\8.0\nios2eds\documents\DBM\_3Cxx.

### *Quartus® II Licensing*

Before you can start to work with this Development Kit you need a license for the Quartus® II Web Edition. The Quartus® II license is based on your computer's network identification card (NIC) ID. To read your NIC number, perform one of the following commands:

- open a DOS-Prompt and type ipconfig /all.  
The NIC ID is the number on the line labelled "Physical Address" without the hyphens. This is a 12 digit value. Using this number, the Altera® homepage (<http://www.altera.com/support/licensing/lic-index.html>) can be used to receive a respecting "Quartus® II Web Edition" license file.
- use the Quartus® II software for the licensing  
After having started the Quartus® II Web Edition, the software asks for a license. Now an automatic license request can be started.

### *Nios® II Licensing*

#### **Licence version**

If you ordered a board with a NIOS II license, this license can be downloaded together with the Quartus Web Edition license from the web.

**You have to provide the same NIC Number for NIOS II with the order of the kit.**

#### **Eval Version**

The Eval Version of the Nios® II allows the complete evaluation and testing of the Nios® II processor including the software tool flow. The restriction of the Eval Version is that the application cannot be programmed into the flash memory.

There are two solutions running a Nios® II Design on the DBM3Cxx Cyclone III NIOS II System Module.

- using an existing Nios® II License or buying an IP-Nios from your local Altera distributor
- using the Open-Core-Plus version of the Nios® II Processor. The Open-Core-Plus Feature allows to run the Nios® II on the hardware with the time-limited version. Generating a new design Quartus® II generates a <project\_name>\_time\_limited.sof file. This file can be downloaded to the board and the applications run until the connection between Quartus® II and the board is terminated. With this feature complete applications can be tested.

### ***Setting up the board***

To setup the board together with the DBM3Cxx\_baseboard, plug the DBM3Cxx module into the baseboard. The connectors are marked, so make sure both parts are fit easily together.

Then connect the USB Blaster with an USB port of your PC and the JTAG connector P1 of the DBM3Cxx Baseboard. Be sure that pin 1 of the USB-Blaster Header fits to pin1 of the board. Figure 2 shows the location of the JTAG connector.

Connect the wall-plug power supply to the baseboard P11. Now the power LED on the module should be on. The baseboard provides a 3.3V to the module. The module generates the 1.2V and 2.5V supply for internal use.

The board can be powered in a range from 5V to 24V with several restrictions:

**For custom designs, make sure that the unused pins are set to input / tri-state. In Quartus®II this option can be set in assignments / device and pin options / unused pins.**

**The Cyclone III FPGAs are not 5V tolerant. Make sure to connect only signals with 3.3V to the pin header.**

### ***Flashing the board***

#### **Programming the configuration device**

To program the EPCS64 configuration device on the DBM3Cxx Nios II System Module, a JTAG indirect programming file (.jic) is used. In the file / convert programming file menu in Quartus®II a .SOF file can be converted into a .jic file. The .jic file can be selected in the Quartus®II programmer (in JTAG mode). Make sure that both configure / program lines are selected to download the loader into the FPGA and the SOF file into the configuration device.

The Nios®II IDE flash programmer can also be used to program a SOF file into the configuration device.

#### **Programming the parallel flash**

For programming the parallel flash the flash programmer of the Nios®II IDE is used. Just start the flash programmer in the tools menu and select the respective project. Then press the program button and the application will be written into the flash device.

### Reference designs

#### Standard

The Standard Reference Design includes a NIOS with SDRAM, SRAM and Flash, a UART, JTAG UART, Timer and IO Ports. A small “hello word” program is included.

#### Gigabit Ethernet Design ALSE

There is a reference Design available for the DBM Modules coming from [www.ALSE-FR.com](http://www.ALSE-FR.com). This Reference Design demonstrates the GEDEK IP-Core from ALSE.

#### Gigabit Ethernet Design IFI

There is a reference Design available for the DBM Modules coming from [www.IFI-PLD.de](http://www.IFI-PLD.de). The design can be downloaded from the IFI homepage, together with the GMAC II IP Core.

#### 10/100Mbit Ethernet Design Maco Engineering

There is a reference Design available for the DBM Modules coming from [www.maco-engineering.de](http://www.maco-engineering.de). The design includes a 10/100Mbit MAC with a respective Ethernet TCP-IP Stack in a 5-in-1 package.

## Board Description

### FPGA Configuration

The JTAG Signals of the DBM3Cxx NIOS II System Module are located on Pin header P2. You should implement an Altera conform JTAG Pin Header for the Altera Programming adapter. The pinout of this connector can be found in the description of the baseboard. To program the Configuration Device a .jic file is required. Refer to Section “Programming the configuration device” in this document.

### Clocking

The DBM3Cxx NIOS II System module includes a free running 25MHz Crystal Quartz Oscillator. The Crystal Quartz Oscillator drives the FPGA and the Ethernet Phy. Table 1

shows the clock distribution on the DBM3Cxx module. The Crystal Quartz Oscillator is a  $\pm 50$ ppm Clock source. The Board delay of the clock line for all clock connections is equal. The On-chip PLLs are used to generate external clocks for the SDRAM, LVDS I/O and application specific I/Os

### Clock Distribution

Function	FPGA Pin	Signal Name
25MHz	A11 (CLK14)	CLK25A
25Mhz	A12 (CLK8)	CLK25A
25MHz	AA12 (CLK13)	CLK25B
25MHz	AB12 (CLK12)	CLK25B
25MHz		CLK25MAC
LVDS Input Clock (+)	G21 (CLK4)	LVDSIN3P
LVDS Input Clock (-)	G22 (CLK5)	LVDSIN3N
SDRAM Clock	T16 (PLL4 out)	SD_CLK
IN0	G2 (CLK0)	GIN0
IN1	G1 (CLK1)	GIN1
IN2	T2 (CLK2)	GIN2
IN3	T1 (CLK3)	GIN3
IN4	T21 (CLK6)	GIN4
IN4	T22 (CLK7)	GIN5
ETX_CLK	AA11 (CLK15)	ETX_CLK
ERX_CLK	AB11 (CLK14)	ERX_CLK
EGTX_CLK	AA3 (PLL1_out)	EGTX_CLK

Table 1

The Crystal Quartz Oscillator supplies 2 PLLs of the FPGA and the Ethernet Phy with a clock of 25MHz. The SDRAM clock is generated with the external output of PLL4. PLL1 generates the 125MHz Ethernet Clock. PLL 2 and 3 can be used for internal clocks.

### SDRAM Clock Setting

The SDRAM Clock is generated from the FPGA PLL Output. The phase of the PLL should be set that

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Offset delay of the PLL – tco of the Clock Signal is between –1.0ns and –2.0ns.

The Offset delay value can be found in the Quartus®II compilation report, Timing Analysis, Clock Setting Summary. The tco can be found in the tco-section.

### Power Supply

The DBM3Cxx NIOSII System Module requires a 3.3V supply. The core voltage (1.2V) and the 2.5V internal I/O voltage are generated on the module.

A Power Good signal is generated for the 1.2V and 3.3V input voltage.

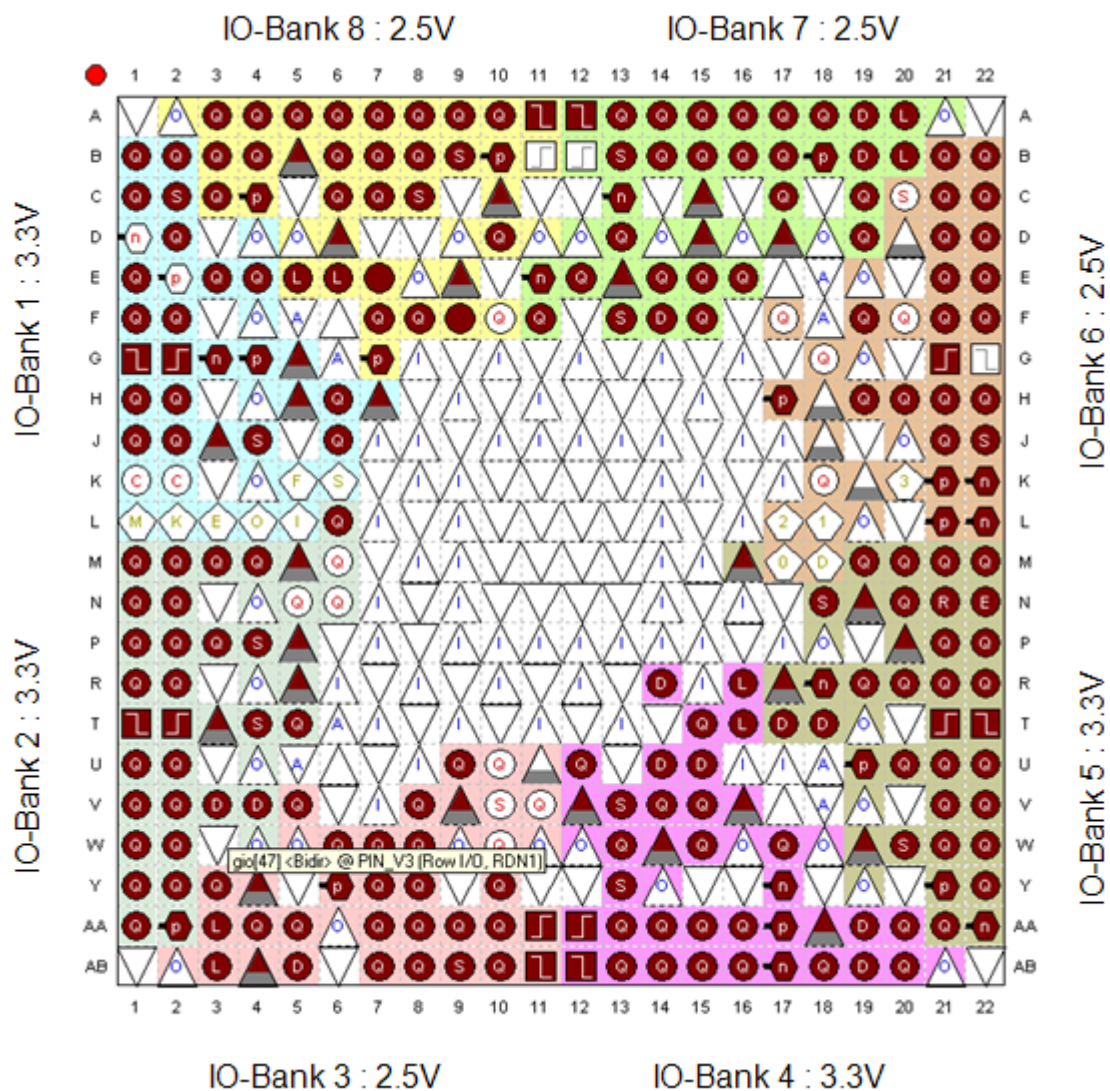


figure 2

## DBM3Cxx – Cyclone III NIOS II System Module

IO-Bank	Used for	Supply
1	GIO	3.3V
2	GIO	3.3V
3	Ethernet Phy	2.5V
4	SDRAM	3.3V
5	SDRAM / GIO	3.3V
6	LVDS	2.5V
7	SRAM / Flash	2.5V
8	SRAM / Flash	2.5V

Table 2

### Reset Signal

Function	Pin	Signal Name
Power Good	U12	RSTn

Table 3

### I/O Connections

#### *Ethernet Phy*

For Ethernet Connectivity a Marvel Gigabit Ethernet PHY is implemented. Table 4 shows the wiring between the FPGA and the 88E1119R. The GMII Interface is used for communication with the FPGA. The LED[0] and LED[1] Outputs of the Phy are connected to the LEDs on the RJ45 connector. LED[2] can be used as IRQ or Link Status and is connected to the FPGA.

There are several Ethernet-MAC IP-Cores available to work together with the 88E1119R Ethernet Phy.

The Phy addresses are set to 0x01 by default. The RXD[4..0] Signals can be used to change the PHYADR. The Phy address Pins are latched with the rising edge of the Phy reset signal.

#### Phy (U9) FPGA Connection

Function	Pin	FPGA Pin
XTAL_IN	41	--
Resetrn	14	U9
RX_CRS	54	AB9
RX_COL	53	AA9
RX_CLK	57	AB11
RX_DV	56	AB8
RX_ERR	55	AA8
RXD0	59	AA7
RXD1	60	AB7
RXD2	61	Y7
RXD3	62	AB5
RXD4	63	AA5
RXD5	64	AB4
RXD6	65	AA4
RXD7	66	AB3
GTX_CLK	6	AA3
TX_CLK	67	AA11
TX_EN	69	V8
TXD0	70	W6
TXD1	71	V5
TXD2	72	V9
TXD3	1	Y3
TXD4	2	W7
TXD5	3	Y6
TXD6	4	W8
TXD7	5	Y4
ECOMAn	8	Y8
MDC	52	AB10
MDIO (Weak Pull-up required)	49	AA10
ELINK (LED2)	13	Y10

## DBM3Cxx – Cyclone III NIOS II System Module

Table 4

### SDRAM

An ISSI 512Mbit SDRAM is used on the DBM3Cxx Nios II System Module. The IS42S32160 Device is a 16Mx32bit SDRAM. Table 5 shows the wiring between the FPGA and the SDRAM. The Clock of the SDRAM comes directly from the FPGA (PLL4).

Figure 3 shows the SDRAM Timing Settings up to 66MHz Design. For more than 66MHz set the CAS latency cycles to 3!

The clock phase for the SDRAM must be set that the sum of PLL Offset and tco for the SDRAM clock signal is about  $-1.2\text{ns}$ . The PLL Offset value can be found in the Quartus compilation report, Timing Analysis, Clock Setting Summary. The tco can be found in the tco-section.

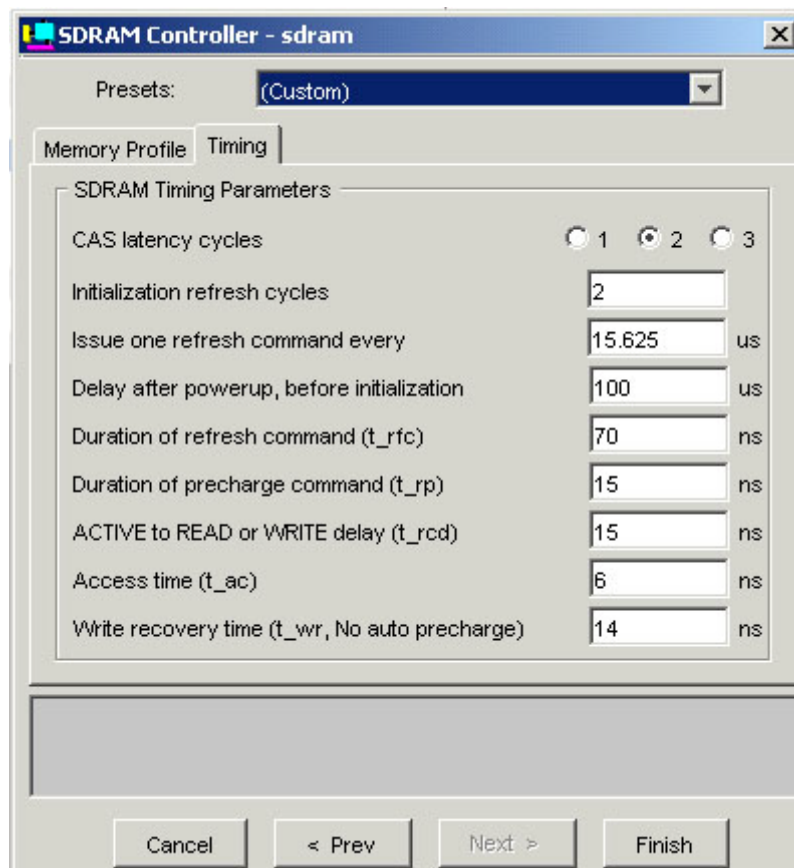


Figure 3

### FPGA Connection

Function	Pin	FPGA Pin
SDCLK	J1	T16
SCKE	J2	R20
SCSn	J8	AA18
SRASn	J9	AB19
SCASn	K7	U20
SWEn	K8	AA19

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Function	Pin	FPGA Pin
SDQM0	K9	AB20
SDQM1	K1	V22
SDQM2	F8	AB16
SDQM3	F2	W17
SA0	G8	AA16
SA1	G9	AB17
SA2	F7	U14
SA3	F3	Y17
SA4	G1	R17
SA5	G2	T15
SA6	G3	U15
SA7	H1	U19
SA8	H2	W19
SA9	J3	W20
SA10	G7	R16
SA11	H9	AB18
SA12	H3	T18
SBA0	J7	R19
SBA1	H8	AA17
SDQ0	R8	Y22
SDQ1	N7	W22
SDQ2	R9	W21
SDQ3	N8	AA22
SDQ4	P9	Y21
SDQ5	M8	AA21
SDQ6	M7	V21
SDQ7	L8	AA20
SDQ8	L2	U21
SDQ9	M3	U22
SDQ10	M2	R21
SDQ11	P1	N21
SDQ12	N2	P21
SDQ13	R1	N22
SDQ14	N3	R22
SDQ15	R2	P22
SDQ16	E8	AA15
SDQ17	D7	V13
SDQ18	D8	AB15
SDQ19	B9	AB14
SDQ20	C8	AA14
SDQ21	A9	AA13
SDQ22	C7	V12
SDQ23	A8	AB13
SDQ24	A2	W13
SDQ25	C3	W15
SDQ26	A1	Y13
SDQ27	C2	W14
SDQ28	B1	V14

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Function	Pin	FPGA Pin
SDQ29	D2	V16
SDQ30	D3	V15
SDQ31	E2	T17

Table 5

### SRAM and Flash

The DBM3Cxx NIOS II System Module is equipped with a 512Kx32bit RAM (U3) and a up to 64Mx16bit Flash (U4). Table 6 shows the wiring between the SRAM / Flash and the FPGA. The Address and Data Signals read and write control signals are shared between Flash and SRAM.

### FPGA Connection

Function	Flash	SRAM	FPGA Pin
FS_A1	E2		E14
FS_A2	D2	G1	F14
FS_A3	C2	G2	F15
FS_A4	A2	H2	C19
FS_A5	B2	H1	D19
FS_A6	D3	G3	C7
FS_A7	C3	H3	C6
FS_A8	A3	J3	D17
FS_A9	B6	H8	E16
FS_A10	A6	H7	B20
FS_A11	C6	J7	D15
FS_A12	D6	G7	C15
FS_A13	B7	F3	A19
FS_A14	A7	K3	A20
FS_A15	C7	J8	A18
FS_A16	D7	H9	B17
FS_A17	E7	G9	A17
FS_A18	B3	J2	F11
FS_A19	C4	G8	C10
FS_A20	D5	F7	E12
FS_A21	D4		D10
FS_A22	C5		E11
FS_A23	B8		B19
FS_A24	C8		B18
FS_A25	F8		B16
FS_A26	G8		B15
FS_CS_FLASHn	F2		F9
FS_CS_RAMn		J9	A7
FS_OEn	G2	K7	F7
FS_WEn	A5	K8	C17
FS_BE0n		F2	E7
FS_BE1n		K1	D6
FS_BE2n		K9	B6
FS_BE3n		F8	B7
FS_D0	E3	B1	C8

## DBM3Cxx – Cyclone III NIOS II System Module

Function	Flash	SRAM	FPGA Pin
FS_D1	H3	A1	E9
FS_D2	E4	E2	F13
FS_D3	H4	C2	F8
FS_D4	H5	D2	A14
FS_D5	E5	C3	C13
FS_D6	H6	D3	B14
FS_D7	E6	A2	E15
FS_D8	F3	P1	C3
FS_D9	G3	N2	E5
FS_D10	F4	R1	B3
FS_D11	G4	N3	G7
FS_D12	F5	M2	E13
FS_D13	G6	M3	A15
FS_D14	F6	L2	D13
FS_D15	G7	R2	A16
FS_D16		R8	B4
FS_D17		R9	A3
FS_D18		P9	A4
FS_D19		N8	C4
FS_D20		N7	A5
FS_D21		M7	E6
FS_D22		M8	B5
FS_D23		L8	A6
FS_D24		E8	A8
FS_D25		D8	A9
FS_D26		D7	B8
FS_D27		C7	B10
FS_D28		C8	B9
FS_D29		B9	A10
FS_D30		A9	B13
FS_D31		A8	A13

Table 6

## DBM3Cxx – Cyclone III NIOS II System Module

### Pin Header

Two 70 pin headers each are connected to the FPGA. Table 7 shows the pinning and the FPGA connection for Pin Header P1. Table 8 shows the pinning and the FPGA connection for Pin Header P2.

The 70 pin Header are SMT Female Header, pitch 1.27mm double row, 6060-070-46-50-10-10 from [www.wppro.com](http://www.wppro.com) or SFM-135-02-S-D-LC from [www.Samtec.com](http://www.Samtec.com).

**Make sure that only 3.3V signals are connected to the Pin Headers P1 and P2.**

### I/O Connector P1

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		GND
VCC33		3	4		VCC33
GND		5	6		GND
LVDS_OUT0P	F19	7	8	B21	LVDS_IN0P
LVDS_OUT0N	F20	9	10	B22	LVDS_IN0N
GND		11	12		GND
LVDS_OUT1P	C21	13	14	D21	LVDS_IN1P
LVDS_OUT1N	C22	15	16	D22	LVDS_IN1N
GND		17	18		GND
LVDS_OUT2P	F21	19	20	E21	LVDS_IN2P
LVDS_OUT2N	F22	21	22	E22	LVDS_IN2N
GND		23	24		GND
LVDS_OUT3P	H17	25	26	H21/G21	LVDS_IN3P
LVDS_OUT3N	G18	27	28	H22/G22	LVDS_IN3N
GND		29	30		GND
LVDS_OUT4P	K21	31	32	J21	LVDS_IN4P
LVDS_OUT4N	K22	33	34	J22	LVDS_IN4N
GND		35	36		GND
LVDS_OUT5P	H19	37	38	L21	LVDS_IN5P
LVDS_OUT5N	H20	39	40	L22	LVDS_IN5N
GND		41	42		GND
GIO50	M22	43	44	M21	GIO51
GIO52	M19	45	46	M20	GIO53
GIO54	P20	47	48	N20	GIO55
GND		49	50		GND
GIN4	T21	51	52	T22	GIN5
GND		53	54		GND
GIO56	N18	55	56	N19	GIO57
GIO58	R18	57	58	M16	GIO59
GIO60	M5	59	60	J3	GIO61
GIO62	T5	61	62	L6	GIO63
VCC33		63	64	R14	GIO64
VCC33		65	66		GND
VCC33		67	68		VCC33
GND		69	70		GND

Table 7

## DBM3Cxx – Cyclone III NIOS II System Module

### I/O Connector P2

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		GND
VCC33		3	4		VCC33
GIO0	E1	5	6	D2	GIO1
GIO2	F2	7	8	C1	GIO3
GIO4	F1	9	10	G5	GIO5
GIO6	H7	11	12	E4	GIO7
GIO8	J6	13	14	C2	GIO9
GIO10	J1	15	16	B2	GIO11
GIO12	H1	17	18	B1	GIO13
GIO14	H2	19	20	H6	GIO15
GIO16	J2	21	22	H5	GIO17
GIO18	E3	23	24	G4	GIO19
GIO20	J4	25	26	G3	GIO21
GIN0	G2	27	28	G1	GIN1
VCC25		29	30		GND
TDO		31	32		TMS
TDI		33	34		TCK
VCC25		35	36		GND
GIO22	M1	37	38	M2	GIO23
GIO24	N1	39	40	M3	GIO25
GIO26	N2	41	42	M4	GIO27
GIO28	P1	43	44	P4	GIO29
GIO30	P2	45	46	P3	GIO31
GIN2	T2	47	48	T1	GIN3
GIO32	R1	49	50	V2	GIO33
GIO34	R2	51	52	W1	GIO35
GIO36	U1	53	54	W2	GIO37
GIO38	U2	55	56	Y1	GIO39
GIO40	V1	57	58	Y2	GIO41
GIO42	AA1	59	60	AA2	GIO43
GIO44	P5	61	62	T4	GIO45
GIO46	R5	63	64	V3	GIO47
GIO48	T3	65	66	V4	GIO49
VCC33		67	68		VCC33
GND		69	70		GND

Table 8

## DBM3Cxx – Cyclone III NIOS II System Module

### Bill of Material

Description	Count	Reference Designator
LED 0805 red	1	D1
R0603_10K	3	R2 R3 R4
R0603_1K	7	R5 R6 R7 R13 R14 R15 R16
R0603_470R	1	R17
R0603_4K7	2	R12 R18
R0603_22R	1	R1
R0603_33R	3	R8 R9 R19
R0603_4K99	1	R20
R0603_300R	2	R10 R11
R0603_4K75	1	R21
L0603_10NH 0.4A	3	L3 L4 L5
C1210_47U 6.3V	4	C23 C25 C27 C28
C1210_10U 16V	9	C2 C47 C49 C53 C55 C55 C57 C59 C61 C64
C0603_2N2	2	C11 C12
C0603_100N	39	C1 C4 C5 C6 C7 C8 C9 C10 C13 C13 C16 C17 C18 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C48 C50 C54 C56 C58 C60 C62 C63
C0603_220N	4	C19 C20 C21 C22
Marvell 88E1119R Gig Phy Avnet Memec	1	U9
Tyco 6605814-5 RJ45 with Magn. Avnet Time	1	P3
BC850B	1	U11
BCP69-16	1	U12
Altera EP3CxxF484C7N EBV Elektronik	1	U1
ISSI IS42S32160C-75BLI EBV Elektronik	1	U5
ISSI IS61WV51232BLL10BLI EBV Elektronik	1	U3
National LM2852XMXA-1.2 EBV Elektronik	1	U8
National LM2825XMXA-2.5 EBV Elektronik	1	U7
LWE-T_1UH 2.7 Würth 744042001	2	L1 L2
TI TPS3103K33DVBR EBV Elektronik	1	U10
XOSC25_2.5V Jauch O25-JO32-B-2.5V-1	1	U6

## DBM3Cxx – Cyclone III NIOS II System Module

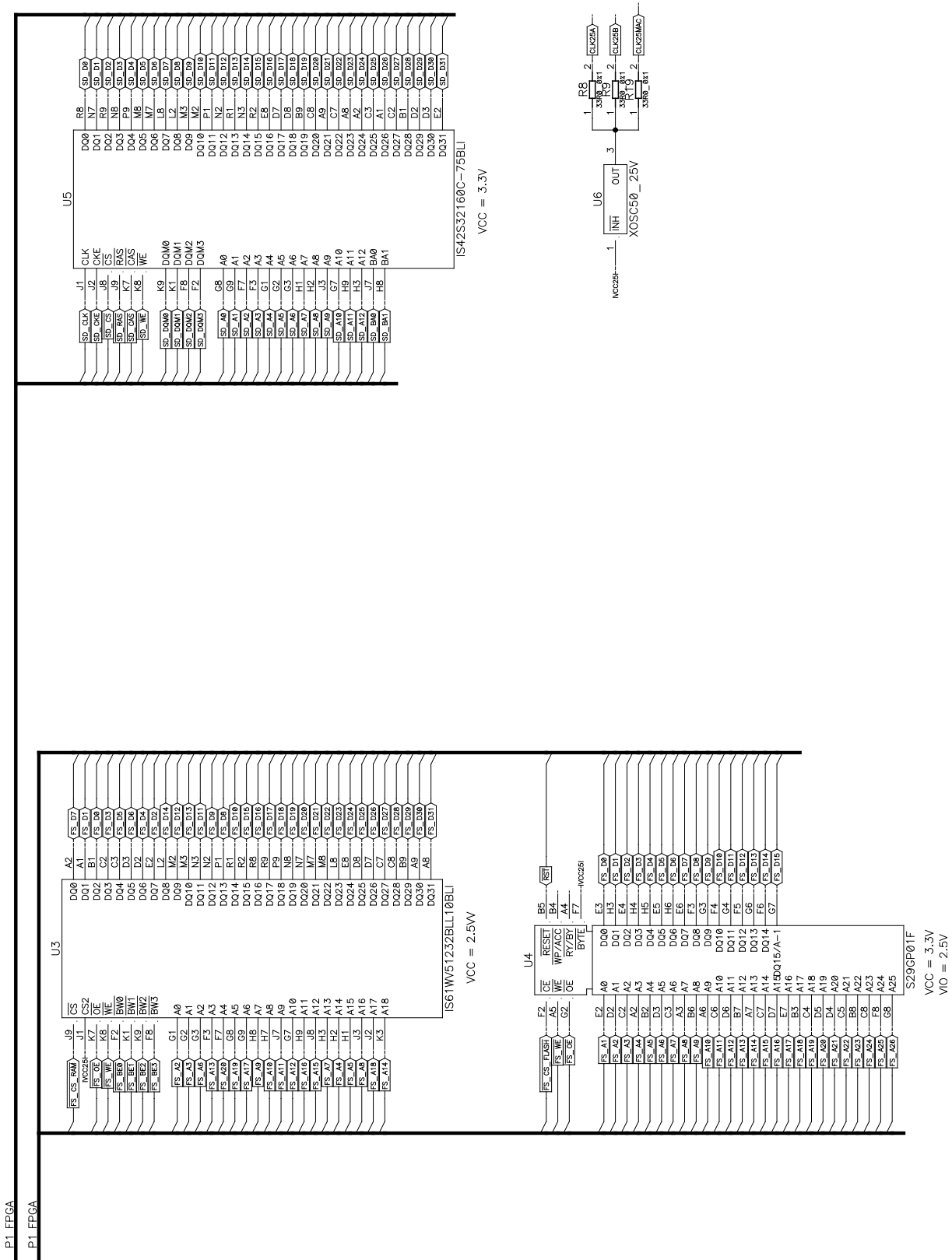
6060-070-46-50-10-10 Avnet Time	2	P1 P2
Altera EPCS64SI16N EBV Elektronik	1	U2
Spansion S29GP01P12FFCR20 EBV Elektronik	1	U4

**Table 9**

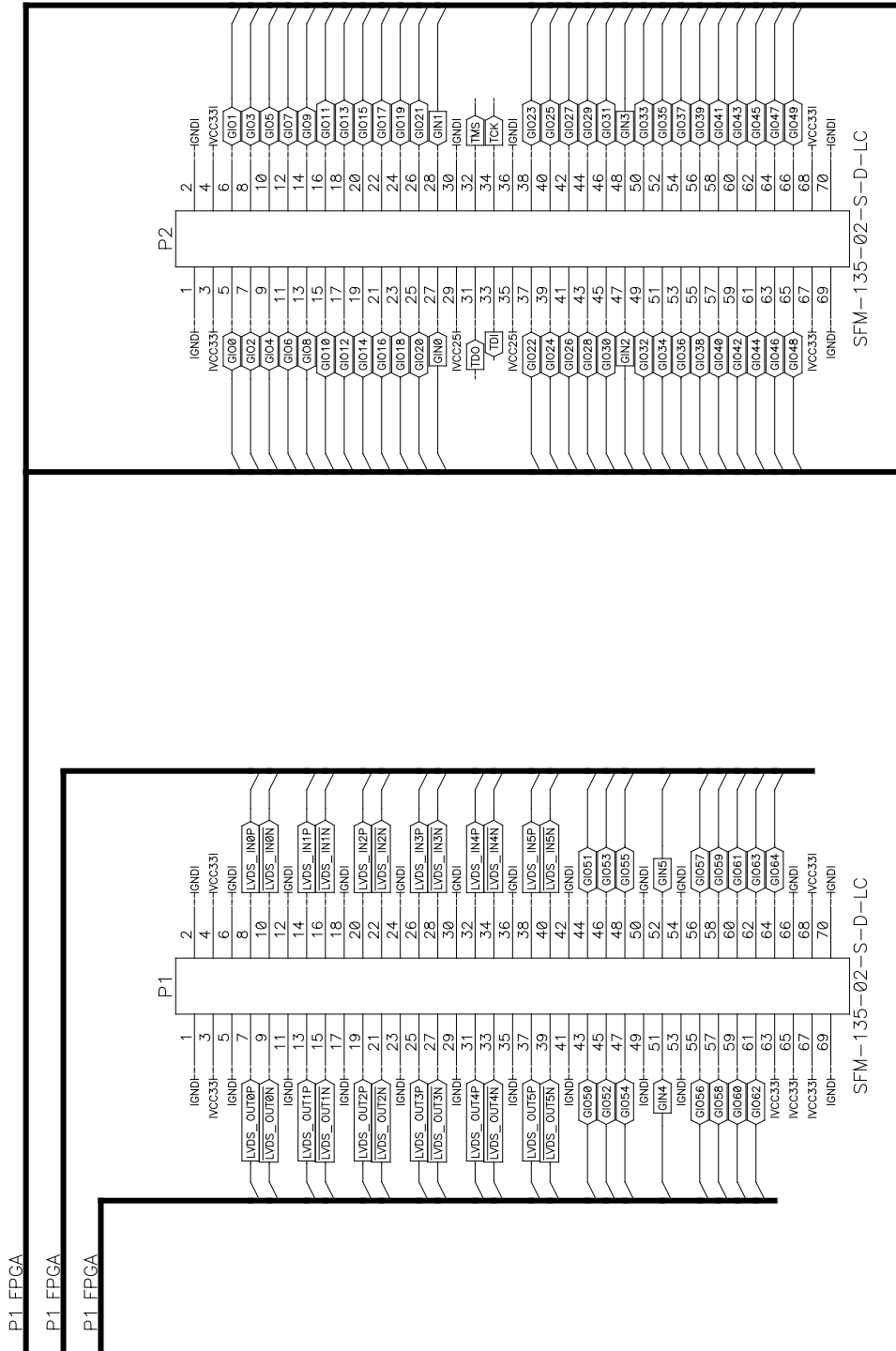


# DBM3Cxx – Cyclone III NIOS II System Module

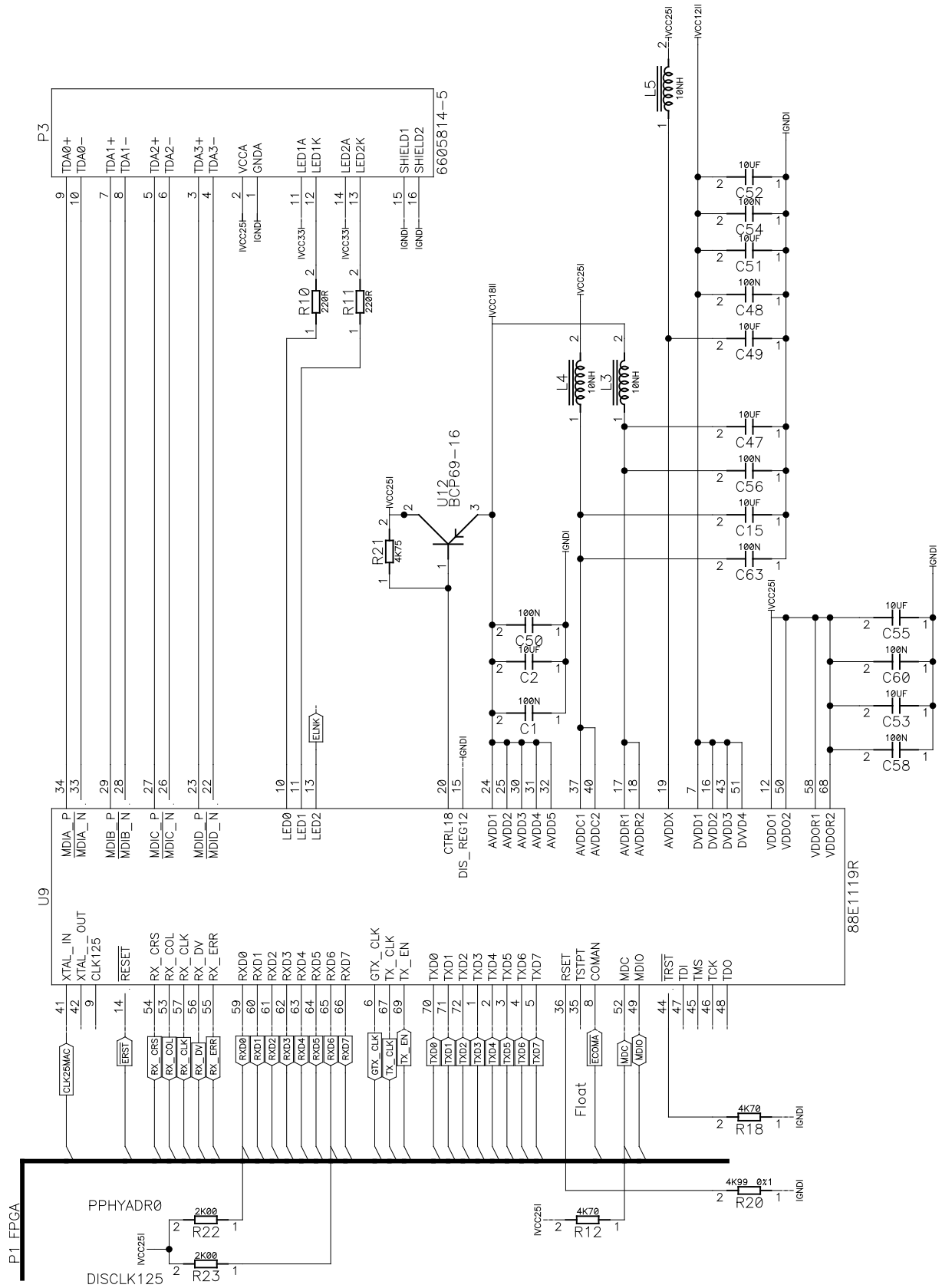
## Memory



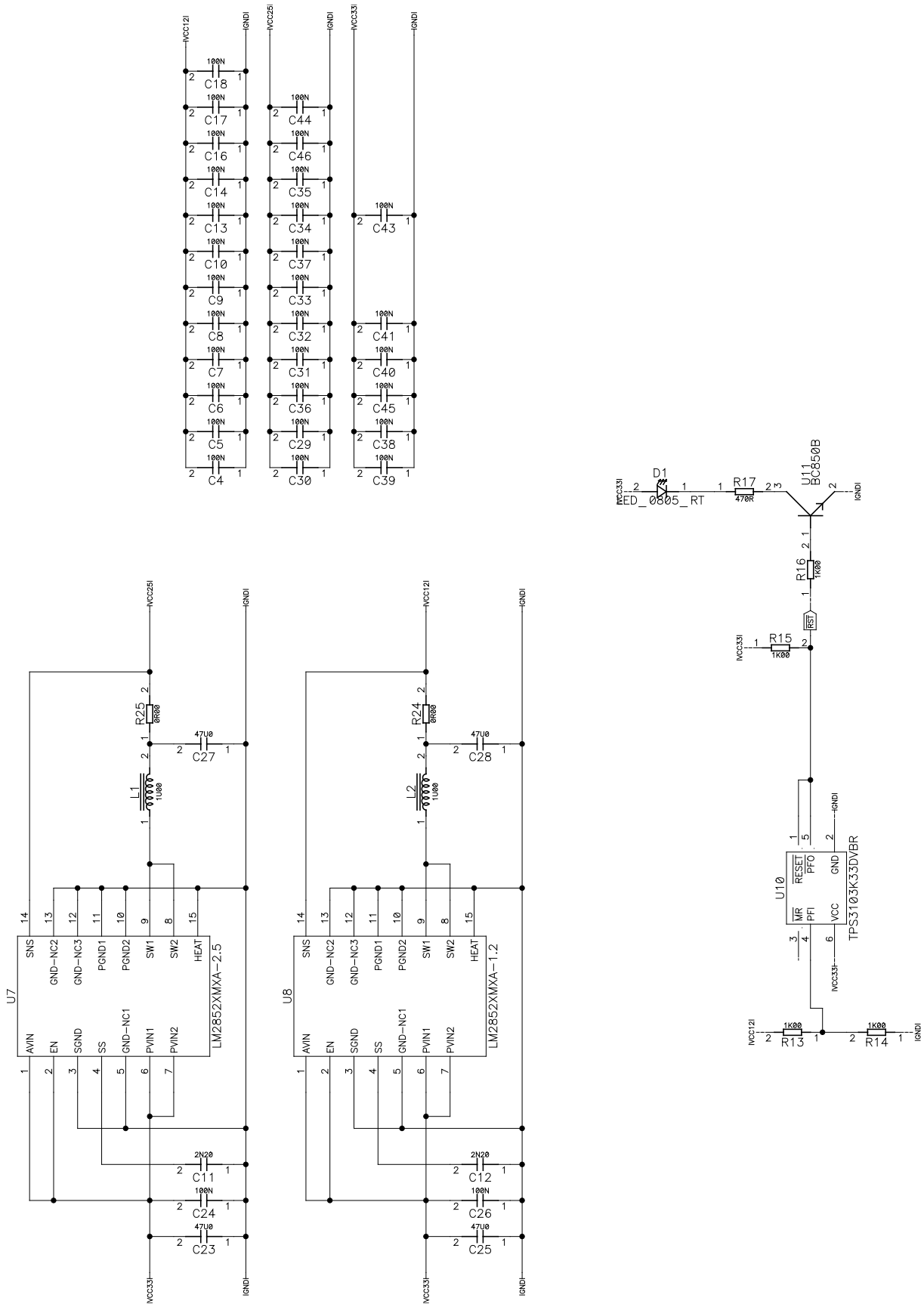
## Interface



## Ethernet



## Power Supply



Board Top View

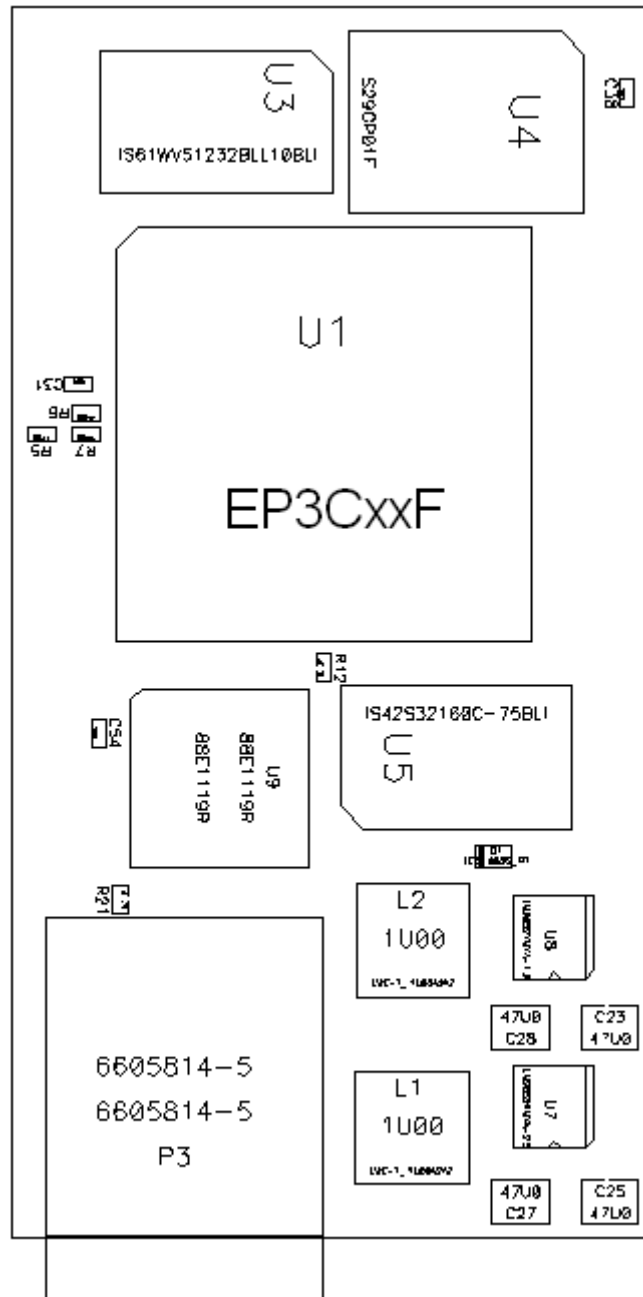


Figure 4

Board Bottom View

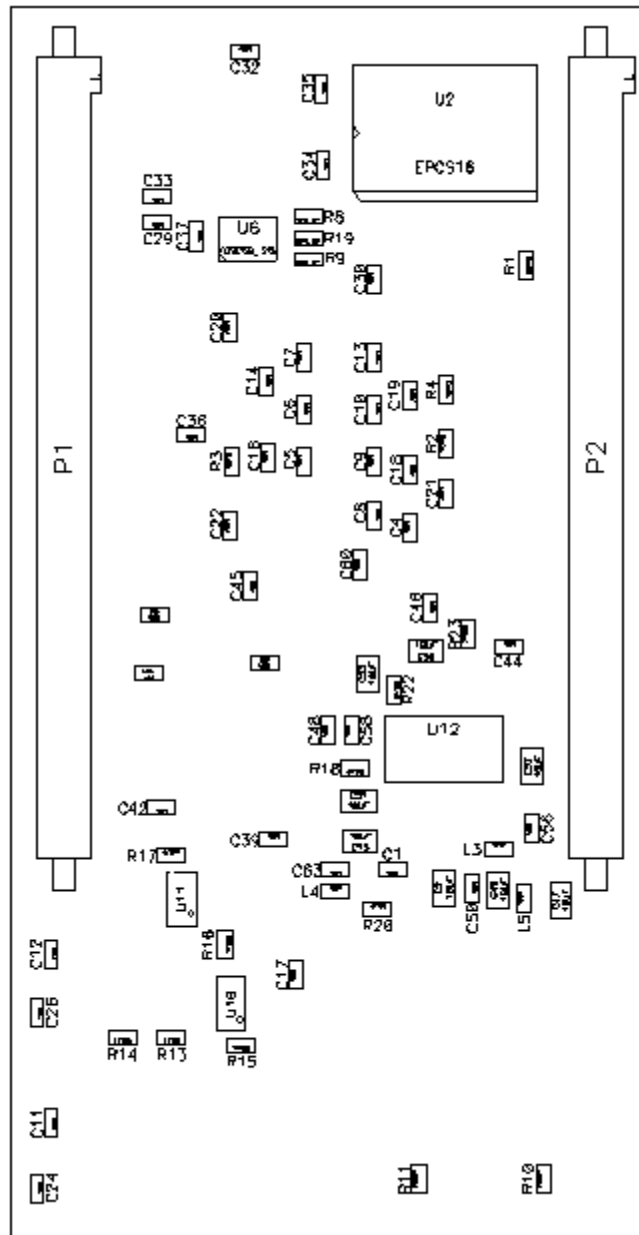


Figure 5

Module Dimension

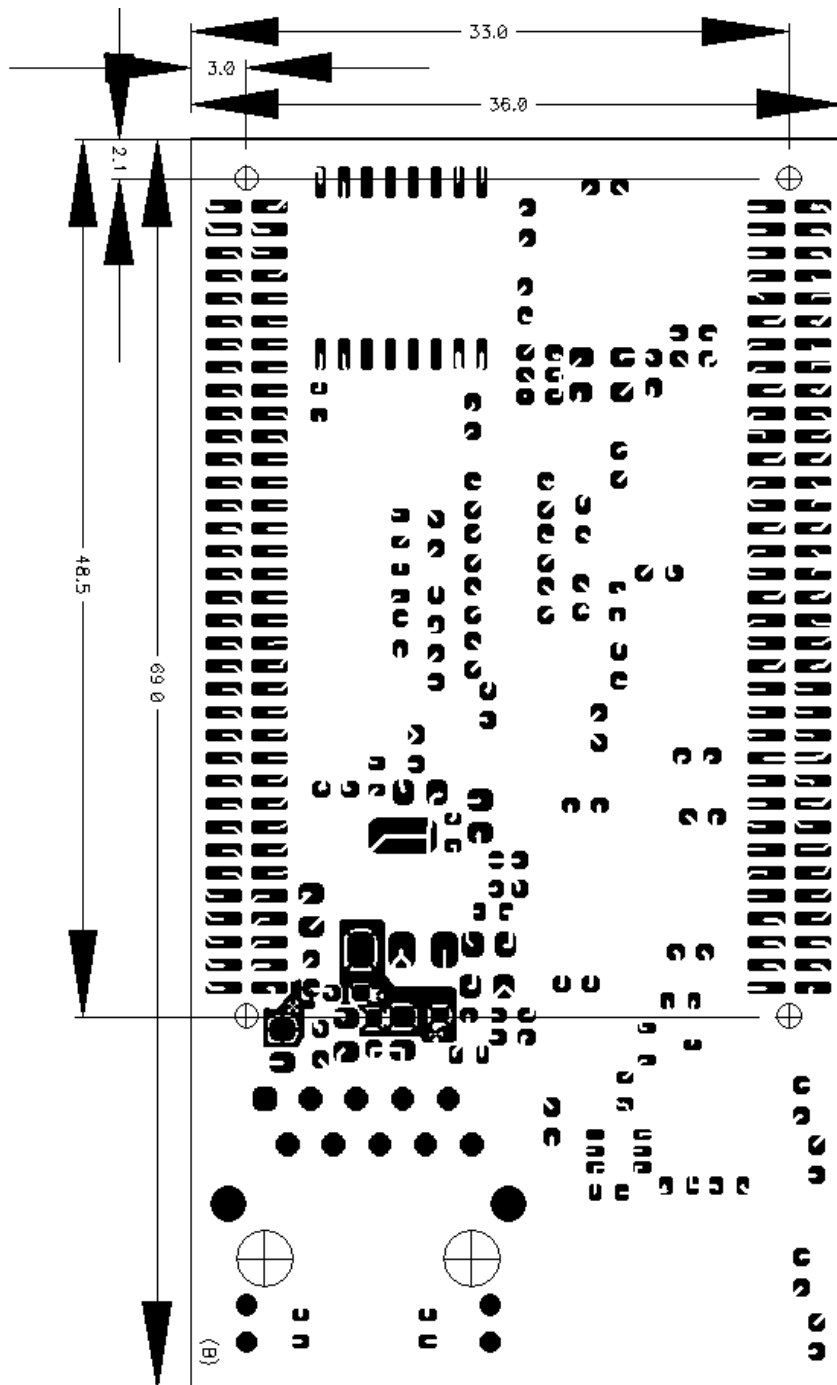


figure 6

### DBM\_CIII\_Base

The DBM\_CIII\_Base contains a power supply for 3.3V and the pin header to contact the module. All Module signals are routed to 2.54mm Pin header to allow an easy connection to the functions. A standard Altera JTAG connector is available too.

A 0.1R Resistor is implemented as a Shunt for current Measurement on the 3.3V Power supply. A Voltmeter can be used to measure the voltage over the shunt. P8 and P9 are Testpoints for the current measurement.

### I/O Connector P4

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		GND
GIO0	E1	3	4	D2	GIO1
GIO2	F2	5	6	C1	GIO3
GIO4	F1	7	8	G5	GIO5
GIO6	H7	9	10	E4	GIO7
GIO8	J6	11	12	C2	GIO9
GIO10	J1	13	14	B2	GIO11
GIO12	H1	15	16	B1	GIO13
GIO14	H2	17	18	H6	GIO15
GIO16	J2	19	20	H5	GIO17
GIO18	E3	21	22	G4	GIO19
GIO20	J4	23	24	G3	GIO21
GIN0	G2	25	26	G1	GIN1
GND		27	28		GND
GIO22	M1	29	30	M2	GIO23
GIO24	N1	31	32	M3	GIO25
GIO26	N2	33	34	M4	GIO27

Table 10

### I/O Connector P5

Function	FPGA	Pin	Pin	FPGA	Function
		1	2		
GND		3	4		GND
LVDS_OUT0P	F19	5	6	B21	LVDS_IN0P
LVDS_OUT0N	F20	7	8	B22	LVDS_IN0N
GND		9	10		GND
LVDS_OUT1P	C21	11	12	D21	LVDS_IN1P
LVDS_OUT1N	C22	13	14	D22	LVDS_IN1N
GND		15	16		GND
LVDS_OUT2P	F21	17	18	E21	LVDS_IN2P
LVDS_OUT2N	F22	19	20	E22	LVDS_IN2N
GND		21	22		GND
LVDS_OUT3P	H17	23	24	H21/G21	LVDS_IN3P
LVDS_OUT3N	G18	25	26	H22/G22	LVDS_IN3N
GND		27	28		GND
LVDS_OUT4P	K21	29	30	J21	LVDS_IN4P

## DBM3Cxx – Cyclone III NIOS II System Module

LVDS_OUT4N	K22	31	32	J22	LVDS_IN4N
GND		33	34		GND
LVDS_OUT5P	H19	35	36	L21	LVDS_IN5P
LVDS_OUT5N	H20	37	38	L22	LVDS_IN5N
GND		39	40		GND

Table 11

### I/O Connector P6

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		GND
GIO50	M22	3	4	M21	GIO51
GIO52	M19	5	6	M20	GIO53
GIO54	P20	7	8	N20	GIO55
GIN4	T21	9	10	T22	GIN5
GIO56	N18	11	12	N19	GIO57
GIO58	R18	13	14	M16	GIO59
GIO60	M5	15	16	J3	GIO61
GIO62	T5	17	18	L6	GIO63
GND		19	20	R14	GIO64
GIO30	P2	21	22	T1	GIN3
GIN2	T2	23	24	R1	GIO32
GIO34	R2	25	26	U1	GIO36
GIO38	U2	27	28	V1	GIO40
GIO42	AA1	29	30	P5	GIO44
GIO46	R5	31	32	T3	GIO48
GND		33	34		GND

Table 12

### I/O Connector P10 (DSUB-9)

Function	FPGA	Pin
		1
RXD (GIO49)	V4	2
TXD (GIO47)	V3	3
		4
GND		5
		6
RTS (GIO45)	T4	7
CTS (GIO43)	AA2	8
		9

Table 13

### I/O Connector P7 (Micro-SD Card)

Function	FPGA	Pin
DATA2 (GIO41)	Y2	1
DATA3 (GIO39)	Y1	2
CMD (GIO37)	W2	3
VCC33		4

## DBM3Cxx – Cyclone III NIOS II System Module

CLK (GIO35)	W1	5
GND		6
DATA0 (GIO33)	V2	7
DATA1 (GIO31)	P3	8
Switch (GIO29)	P4	9

Table 14

### User LED

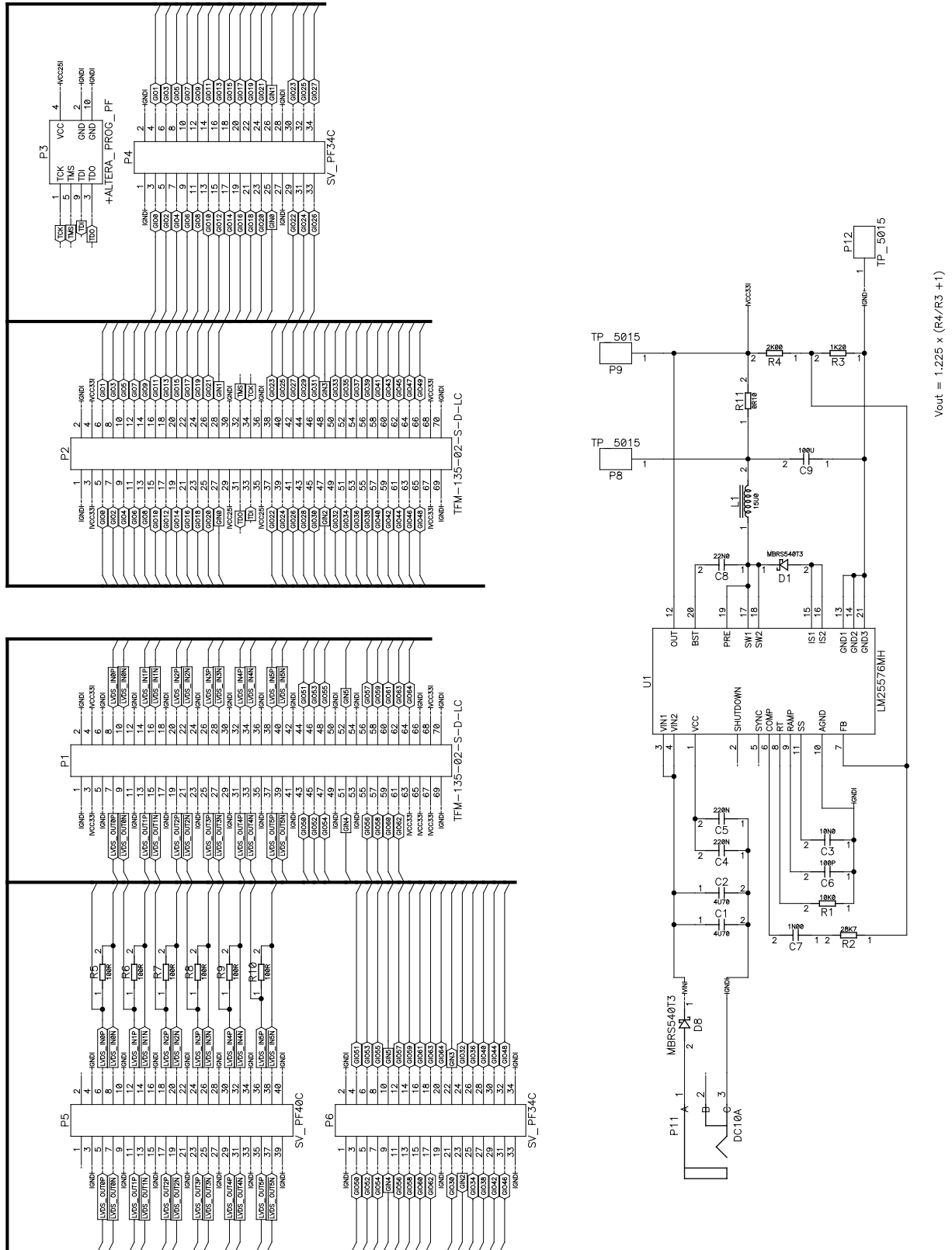
Function	FPGA
LED (GIO28)	P1

Table 15

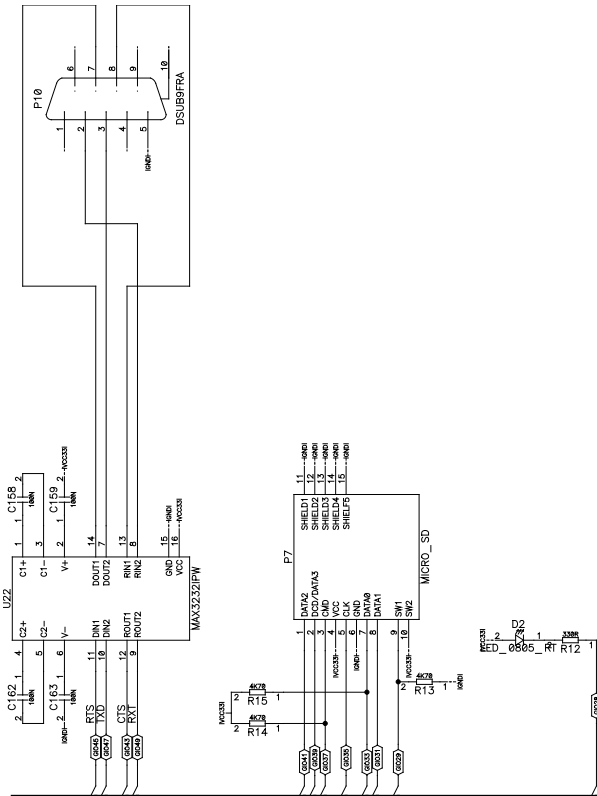
### Bill of Material

Description	Count	Reference Designator
LED 0805 red	1	D2
R0603_10K	1	R1
R0603_100R	6	R5 R6 R7 R8 R9 R10
R0603_330R	1	R12
R0603_2K	1	R4
R0603_4K7	3	R13 R14 R15
R0603_1K2	1	R3
R0603_28K7	1	R2
R2512_0R1	1	R11
C0603_10N	1	C3
C0603_100P	1	C6
C0603_22N	1	C8
C0603_100N	4	C158 C159 C162 C163
C1210_4U7 50V	2	C1 C2
C0603_1N	1	C7
C0603_220N	2	C4 C5
C1210_100U 6V3	1	C9
DC10A	1	P11
DSUB9 (female)	1	P10
Pin 2x5	1	P3
Pin 2x17	2	P4 P6
Pin 2x20	1	P5
Micro SD Farnell #1366700	1	P7
TP SMD	3	P8 P9 P12
National LM25576MH EBV Elektronik	1	U1
TI MAX3232IPW EBV Elektronik	1	U22
MBRS540T3	2	D1 D8
LWE-TL15U 3A6 Würth 744066100	1	L1
Samtec TFM-135-02-S-D-LC	2	P1 P2

## Schematic



## Schematic SD-Card, UART



# DBM3Cxx – Cyclone III NIOS II System Module

## Board top View

